UNITRODE

UCC 3800/1/2/3/4/5 BiCMOS CURRENT MODE CONTROL ICs

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INTRODUCTION

Power supply design has become increasingly more challenging as engineers confront the difficulties of obtaining higher power density, improved performance and lower cost. The control for many of these switchmode supplies was revolutionized with two significant introductions; an advance technique known as current mode control, and a novel PWM solution, the UC3842 controller. This IC contained several innovative features for general purpose current mode controlled applications. Included were high speed circuitry, undervoltage lockout, an op-amp type error amplifier, fast overcurrrent protection, a precision reference and a high current totem-pole output.

The popular UC3842 control circuit architecture has been recently improved upon to deliver even higher levels of protection and performance. Advanced circuitry such as leading edge blanking of the current sense signal, soft-start and full cycle restart have been built-in to minimize external parts count. Additionally, these integrated circuits have been developed on a BiCMOS wafer fabrication process geared to virtually eliminate supply power and propagation delays in comparison to the bipolar UC3842 devices. These sophisticated new BiCMOS controllers, the UCC3800 through UCC3805 pulse width modulators address the challenges presented by the upcoming generations of power supply designs. This application note will highlight the features incoporated into this new generation of PWM controllers in addition to realizeable enhancements in typical applications. The specific differences between members of the UCC3800/1/2/3/4/5 family are reflective of their maximum duty cycle, undervoltage lockout thresholds and reference voltage which are summarized in the following table.

Unitrode Part #	Max Duty Cycle	VRef (V)	UVLO Turn-On	UVLO Turn-Off
UCC3800	100%	5.0	7.2	6.9
UCC3801	50%	5.0	9.4	7.4
UCC3802	100%	5.0	12.5	8.4
UCC3803	100%	4.0	4.1	3.6
UCC3804	50%	5.0	12.5	8.4
UCC3805	50%	4.0	4.1	3.6

UCC3800/1/2/3/4/5 PWM FEATURES

A. Low start-up current
B. Undervoltage lockout
C. Low operating current
D. Internal soft start
E. Self biasing output during UVLO
F. Leading Edge Blanking
G. Self regulating Vcc supply
H. Full cycle restart after fault
I. Clamped gate drive amplitude
J. Reduced propagation delays
K. 5 Volt operation (UCC3803 & 05)

IN-CIRCUIT ADVANTAGES vs. UC3842

- Greatly reduced power requirements
- Eliminates bootstrap supply
- Fewer external components
- Lower junction temperature
- Reduced stress during faults
- No current sense R/C filter network
- Faster response to fault
- Higher frequency operation
- Higher maximum duty cycles

UCC3800/1/2/3/4/5 DEVICE OVERVIEW

The BiCMOS UCC3800/1/2/3/4/5 devices have similar standard features and pinouts to the bipolar UC3842/3/4/5 PWMs and are enhanced replacements in many applications. There are a few important differences however which may require minor modifications to existing applications.

APPLICATION DIFFERENCES

1. Maximum supply voltage from a low impedance source: 12V versus 30V
2. Undervoltage lockout thresholds
3. Start-up current
4. Operating current
5. Oscillator timing component values
6. Reference voltage (UCC3803 and 05)
7. Vcc supply self clamping zener voltage
8. Internal soft start
9. Internal full cycle restart
10. Clamped gate drive voltage
11. Current loop gain
12. E/A reference voltage (’03 & ’05)

UCC3800/1/2/3/4/5 BLOCK DIAGRAM

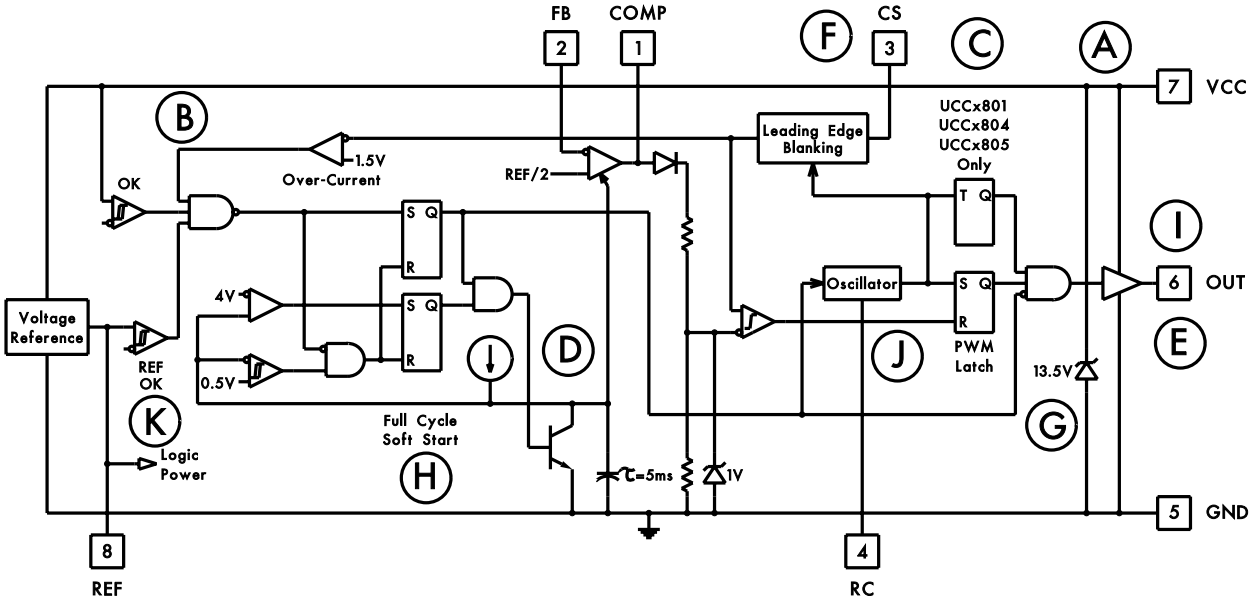

Figure 1.

SUPPLYING POWER

An internal Vcc shunt regulator is incorporated in each member of the UCC3800/1/2/3/4/5 PWMs to regulate the supply voltage at approximately 13.5 volts. A series resistor from Vcc to the input supply source is required with inputs above 12 volts to limit the shunt regulator current as shown in figure 2. A maximum of 10 milliamps can be shunted to ground by the internal regulator.

The internal regulator in conjunction with the device's low startup and operating current can greatly simplify powering the device and may eliminate the need for a regulated bootstrap auxiliary supply and winding in many applications. The supply voltage is MOSFET gate level compatible and needs no external zener diode or regulator protection with a current limited input supply. The UVLO start-up threshold is 1.0 volts below the shunt regulator level on the '02 and '04 devices to guarantee start-up.

It is important to bypass the ICs supply (Vcc) and reference voltage (Vref) pins with a 0.1uF to 1uF ceramic capacitor to ground. The capacitors should be located as close to the actual pin connections as possible for optimal noise filtering. A second, larger filter capacitor may also be required in off-line applications to hold the supply voltage (Vcc) above the UVLO turn-off threshold during start-up.

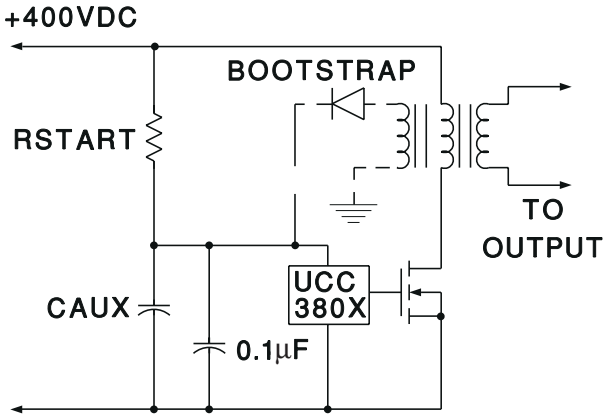

Figure 2. Powering the UCC3802.

UNDERVOLTAGE LOCKOUT

The UCC3800/1/2/3/4/5 devices feature undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. Both the supply voltage (Vcc) and the reference voltage (Vref) are monitored by the UVLO circuitry. An active low, self biasing totem pole output during UVLO design is also incorporated for enhanced power switch protection.

Undervoltage lockout thresholds for the UCC 3802/3/4/5 devices are different from the previous generation of UC3842/3/4/5 PWMs. Basically, the thresholds are optimized for two groups of applications; off-line power supplies and DC-DC converters. The UCC3802 and UCC3804 feature typical UVLO thresholds of 12.5V for turn-on and 8.3V for turn-off, providing 4.3V of hysteresis. For low voltage inputs which include battery and 5V applications, the UCC3803 and UCC3805 turn on at 4.1V and turn off at 3.6V with 0.5V of hysteresis. The UCC3800 and UCC3801 have UVLO thresholds optimized for automotive and battery applications.

During UVLO the IC draws approximately 100 microamps of supply current. Once crossing the turn-on threshold the IC supply current increases typically to about 500 microamps, over an order of magnitude lower than bipolar counterparts.

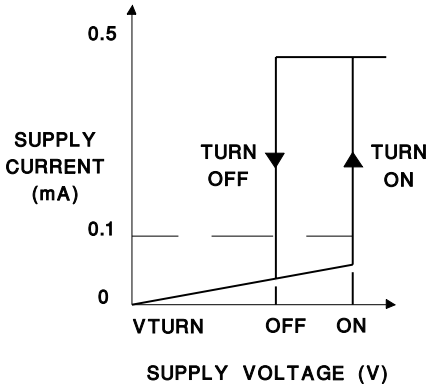

Figure 3. During Undervoltage Lockout

Device	Vton	Vtoff
UCC3800	7.2	6.9
UCC3801	9.4	7.4
UCC3802, 4	12.5	8.3
UCC3803, 5	4.1	3.6

SELF BIASING, ACTIVE LOW OUTPUT

The self biasing, active low clamp circuit shown eliminates the potential for problematic MOSFET turn on. As the PWM output voltage rises while in UVLO, the P device drives the larger N type switch ON which clamps the output voltage low. Power to this circuit is supplied by the externally rising gate voltage, so full protection is available regardless of the ICs supply voltage during undervoltage lockout.

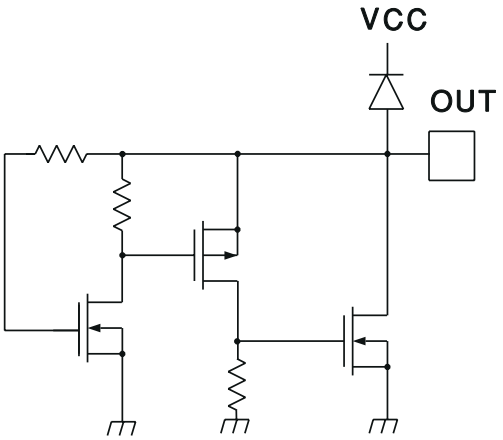

Figure 4: Internal circuit which holds output low during UVLO.

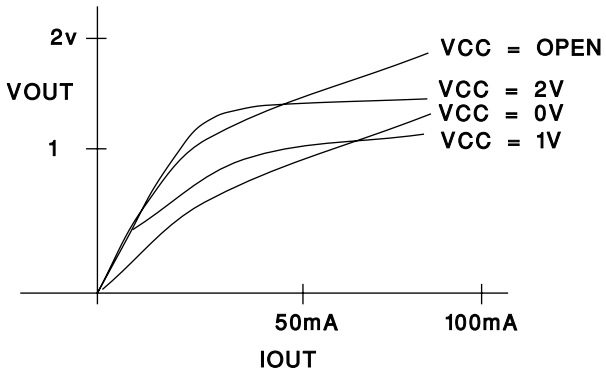

Figure 5: Output voltage vs. output current during UVLO.

REFERENCE VOLTAGE

The traditional 5.0V amplitude bandgap reference voltage of the UC3842 family can be also found on the UCC3800,1,2 and UCC3804 devices. However, the reference voltage of the UCC3803 and UCC3805 device is 4.0 volts. This change was necessary to facilitate operation with input supply voltages below five volts. Many of the reference voltage specifications are similar to the UC3842 devices although the test conditions have been changed, indicative of lower current PWM applications. Similar to their bipolar counterparts, the BiCMOS devices internally pull the reference voltage low during UVLO which can be used as a UVLO status indication.

REFERENCE DIFFERENCES

Note that the 4V reference voltage on the UCC3803 and UCC3805 is derived from the supply voltage (Vcc) and requires about 0.5V of headroom to maintain regulation. Whenever Vcc is below approximately 4.5V, the reference voltage also will drop outside of its specified range for normal operation. The relationship between Vcc and Vref during this excursion is shown in Figure 7.

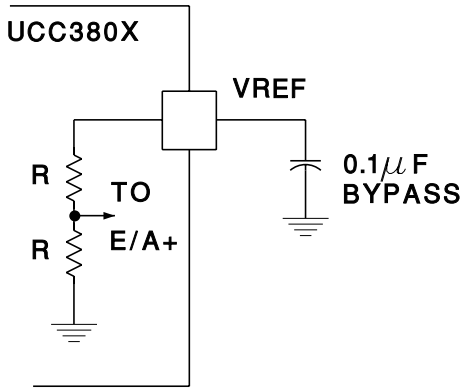

Figure 6: Required reference bypass.

The noninverting input to the error amplifier is tied to one-half of the PWMs reference voltage, Vref. Note that this input is 2.0V on the UCC3803 and UCC3805 and 2.5V on the higher reference voltage parts, the UCC3800, UCC3801, UCC3802 and UCC3804.

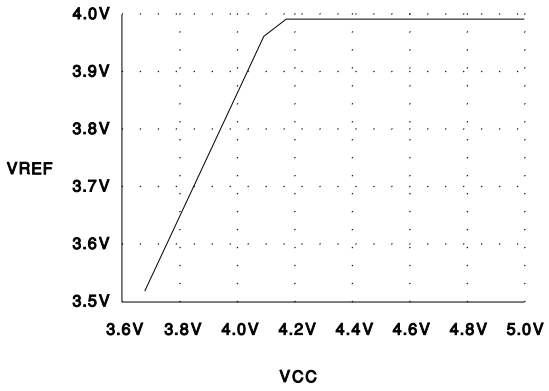

Figure 7: UCC3803 VREF output vs. VCC.

OSCILLATOR SECTION

The oscillator section of the UCC3800 through UCC3805 BiCMOS devices has few similarities to the UC3842 type — other than single pin programming. It does still utilize a resistor to the reference voltage and capacitor to ground to program the oscillator frequency up to 1 MHz. Timing component values will need to be changed since a much lower charging current is desirable for low power operation.

Several characteristics of the oscillator have been optimized for high speed, noise immune operation. The oscillator peak to peak amplitude has been increased to 2.45V typical versus 1.7V on the UC 3842 family. The lower oscillator threshold has been dropped to approximately 0.2 volts while the upper threshold remains fairly close to the original 2.8 volts at approximately 2.65V.

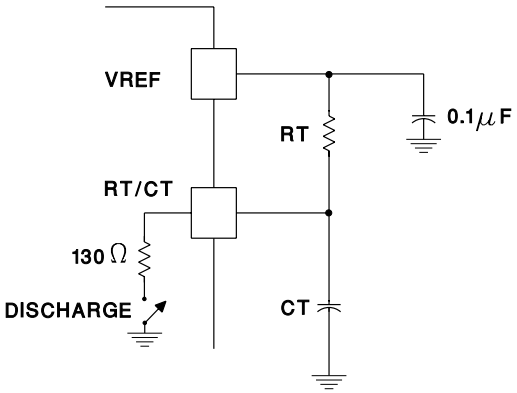

Figure 8: Oscillator equivalent circuit.

Discharge current of the timing capacitor has been increased to nearly 20 milliamps peak as opposed to roughly 8mA. As shown, this can be represented by approximately 130 ohms in series with the discharge switch to ground. A higher current was necessary to achieve brief deadtimes and high duty cycles with high frequency operation. Practical applications can utilize these new ICs to a 1 MHz switching frequency.

SYNCHRONIZATION

Synchronization of these PWM controllers is best obtained by the universal technique shown in figure 12. The ICs oscillator is programmed to free run at a frequency about 20% lower than that of the synchronizing frequency. A brief positive pulse is applied across the 50Ω resistor to force synchronization. Typically, a one volt amplitude pulse of 100 nanoseconds width is sufficient for most applications.

The ICs can also be synchronized to a pulse train input directly to the oscillator Rt/Ct pin. Note that the IC will internally pull low at this node once the upper oscillator threshold is crossed. This 130 ohm impedance to ground remains active until the pin is lowered to approximately 0.2 V. External synchronization circuits should accommodate these conditions.

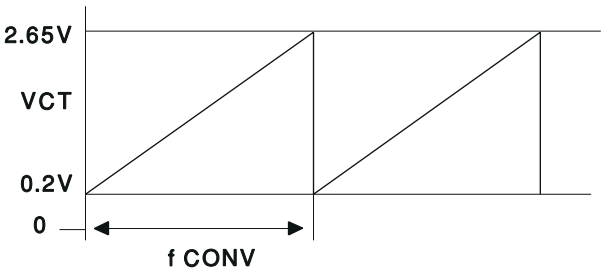

Figure 9: OSC Waveform

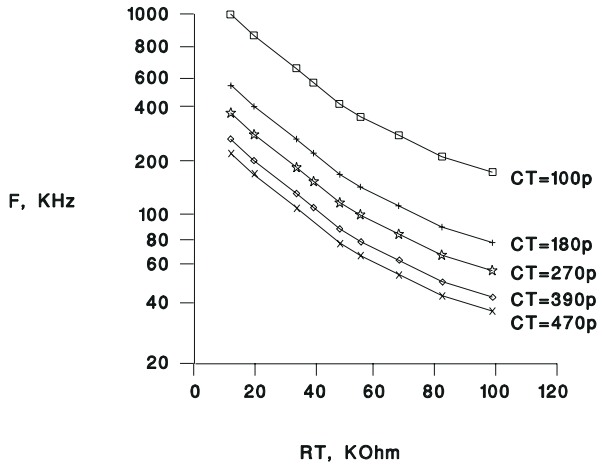

Figure 10: Oscillator frequency vs. RT for several CT.

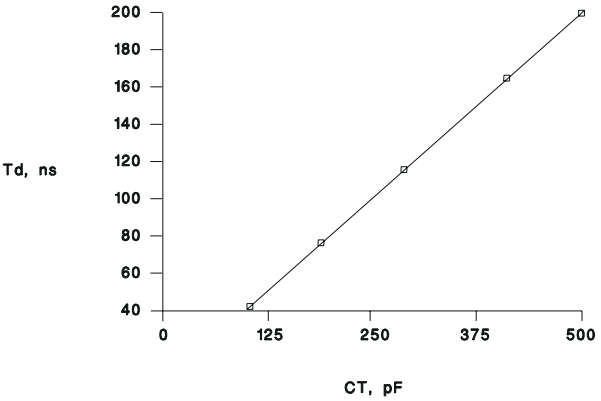

Figure 11: Minimum dead time vs. CT.

PWM SECTION : MAXIMUM DUTY CYCLE

Maximum duty cycle is higher for these devices than for their UC3842/3/4/5 predecessors. This is primarily due to the higher ratio of timing capacitor discharge to charge current which can exceed one-hundred to one in a typical BiCMOS application. **Attempts to program the oscillator maximum duty cycle much below the specified range by adjusting the timing component values of Rt and Ct should be avoided.** There are two reasons to refrain from this design practice. First, the ICs high discharge current would necessitate higher charging currents than necessary for programming,

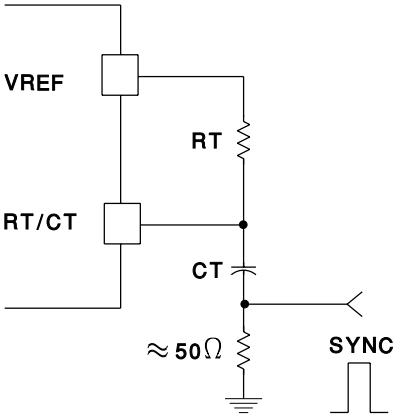

Figure 12: Synchronizing the oscillator.

defeating the purpose of low power operation. Secondly, a low value timing resistor will prevent the capacitor from discharging to the lower threshold and initiating the next switching cycle.

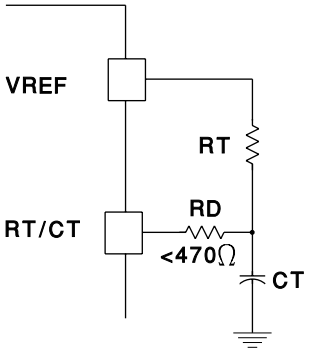

Figure 13: Circuit to produce controlled maximum duty cycle.

DEADTIME CONTROL

Deadtime is the term used to describe the guaranteed OFF time of the PWM output during each oscillator cycle. It is used to insure that even at maximum duty cycle, there is enough time to reset the magnetic circuit elements, and prevent saturation.

The deadtime of the UCC380x PWM family is determined by the internal 130 Ohm discharge impedance and the timing capacitor value. Larger capacitance values extend the deadtime whereas smaller values will result in higher maximum duty cycles for the same operating frequency. A curve for deadtime versus timing capacitor values is provided in figure 11.

Increasing the deadtime is possible by adding a resistor between the Rt/Ct pin of the IC and the timing components. The deadtime increases with the discharge resistor value to about 470 Ohms as indicated from the curve. Higher resistances should be avoided as they can decrease the deadtime and reduce the oscillator peak-to-peak amplitude. Sinking too much current (1 mA) by reducing Rt will "freeze" the oscillator OFF by preventing discharge to the lower comparator threshold voltage of 0.2 V.

Reducing the maximum duty cycle can be accomplished by adding a discharge resistor (below 470 Ohms) between the ICs Rt/Ct pin and the actual Rt/Ct components. Adding this discharge control resistor has several impacts on the oscillator programming. First, it introduces a DC offset to the capacitor during the discharge – but not the charging portion of the timing cycle, thus lowering the usable peak-to-peak timing capacitor amplitude.

Because of the reduced peak-to-peak amplitude, the exact value of Ct may need to be adjusted from UC3842 type designs to obtain the correct initial oscillator frequency. One alternative is keep the same value timing capacitor and adjust both the timing and discharge resistor values since these are readily available in finer numerical increments.

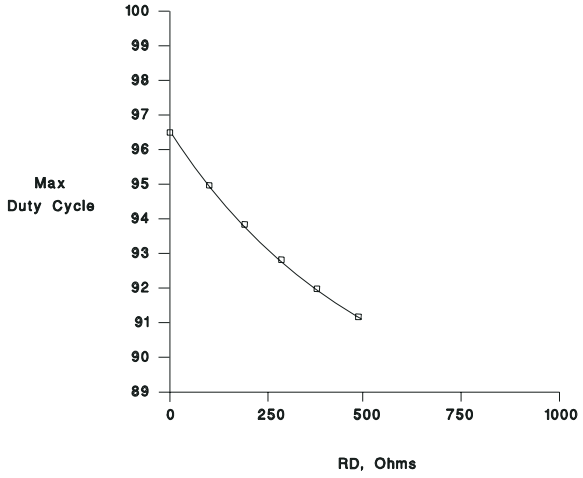

Figure 14: Maximum duty cycle vs. RD for RT = 20k.

LEADING EDGE BLANKING

A 100 nanosecond leading edge blanking interval is applied to the current sense input circuitry of the UCC3800/1/2/3/4/5 devices. This internal feature has been incorporated to eliminate the need for an external resistor-capacitor filter network to sup-

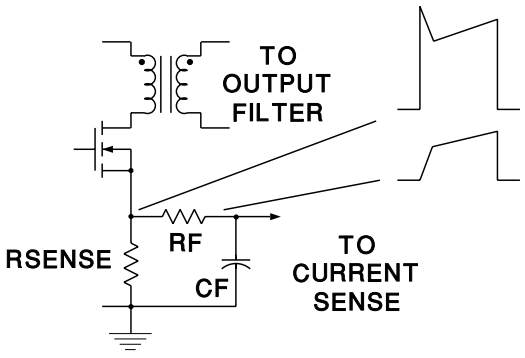

Figure 15: Current sense filter required with older PWM ICs.

press the switching spike associated with turn-on of the power MOSFET. This 100 nanosecond period should be adequate for most switchmode designs but can be lengthened by adding an external R/C filter.

Note that the 100 ns leading edge blanking is also applied to the cycle-by-cycle current limiting function in addition to the overcurrent fault comparator.

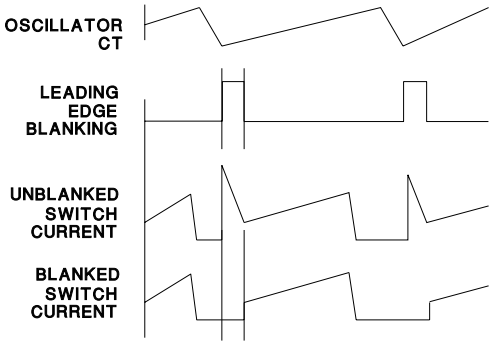

Figure 16: Current sense waveforms with leading edge blanking.

MINIMUM PULSE WIDTH

The leading edge blanking circuitry can lead to a minimum pulse width equal to the blanking interval under certain conditions. This will occur when the error amplifier output voltage (minus a diode drop and divided by 1.65) is lower than the current sense input. However, the amplifier output voltage must also be higher than a diode forward voltage drop of about 0.5V. It is only during these conditions that a minimum output pulse width equal to the blanking duration can be obtained.

Note that the PWM comparator has two inputs; one is from the current sense input. The other PWM input is the error amplifier output which has a diode and two resistors in series to ground. The diode in this network is used to guarantee that zero duty cycle can be reached. Whenever the E/A output falls below a diode forward voltage drop, no current flows in the resistor divider and the PWM input goes to zero, along with pulse width.

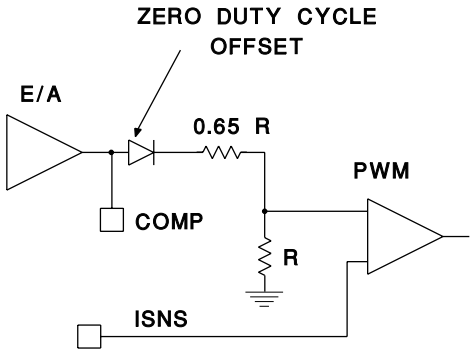

Figure 17.

Zero duty cycle is achievable by forcing the error amplifier output below the zero duty cycle threshold of one diode voltage drop.

PROTECTION CIRCUITRY: CURRENT LIMITING

A 1.0 volt (typical) cycle-by-cycle current limit threshold is incorporated into the UCC3800 family. Note that the 100 nanosecond leading edge blanking pulse is applied to this current limiting circuitry. The blanking overrides the current limit comparator output to prevent the leading edge switch noise from triggering a current limit function.

Propagation delay from the current limit comparator to the output is typically 70 nanoseconds. This high speed path minimizes power semiconductor dissipation during an overload by abbreviating the on time.

CURRENT SENSE OFFSET CIRCUITRY

For increased efficiency in the current sense circuitry, the circuit shown in figure 18 can be used. Resistors RA and RB bias the actual current sense resistor voltage up, allowing a small current sense amplitude to be used. This circuitry provides current limiting protection with lower power loss current sensing.

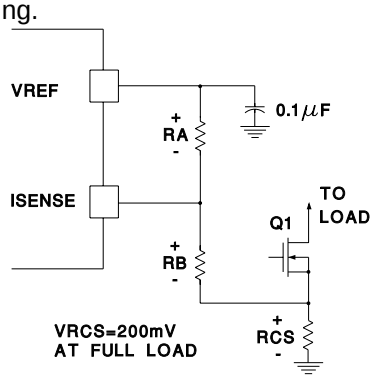

Figure 18: Biasing Isense for lower current sense voltage.

The example shown uses a 200 millivolt full scale signal at the current sense resistor. Resistor Rb biases this up by approximately 700 mV to mate with the 0.9V minimum specification of the current limit comparator of the IC. The value of resistor Ra changes with the specific IC used, due to the different reference voltages. The resistor values should be selected for minimal power loss. For example, a 50 uA bias sets Rb = 13k ohms, Ra=75 k ohms (UCC3800,1,2,4) or Ra=56k ohms with the UCC3803 and UCC3805 devices.

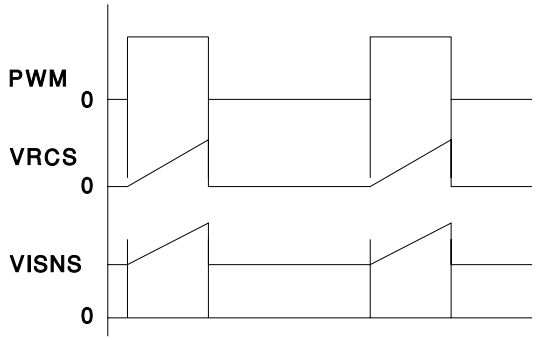

Figure 19.

OVERCURRENT PROTECTION AND FULL CYCLE RESTART

A separate overcurrent comparator within the UCC 3800/1/2/3/4/5 devices handles operation into a short circuited or severely overloaded power supply output. This overcurrent comparator has a 1.5 volt threshold and is also gated by the leading edge blanking signal to prevent false triggering. Once triggered, the overcurrent comparator uses the internal soft start capacitor to generate a delay before retry is attempted. Often referred to as “hiccup”, this delay time is used to significantly reduce the input and dissipated power of the main converter and switching components.

Full Cycle Soft Start insures that there is a predictable delay of greater than 3 milliseconds between successive attempts to operate during fault. The circuit shown in figure 20 and the timing diagram in figure 21 show how the IC responds to a severe fault, such as a saturated inductor. When the fault is first detected, the internal soft start capacitor instantly discharges and stays discharged until the fault clears. At the same time, the PWM output is turned off and held off. When the fault clears, the capacitor will slowly charge and will allow the error amp output (COMP) to rise. When COMP gets high enough to enable the ouput, another fault occurs, latching off the PWM output, but the soft start capacitor still continues to rise to 4V before being discharged and permitting start of a new cycle. This means that for a severe fault, sucessive retries will be spaced by the time required to fully charge the soft start capacitor.

Low leakage transformer designs are recommended in high frequency applications to activate the overcurrent protection feature. Otherwise, the switch current may not ramp up sufficiently to trigger the overcurrent comparator within the leading edge blanking duration. This condition would cause continual cyclical triggering of the cycle-by-cycle

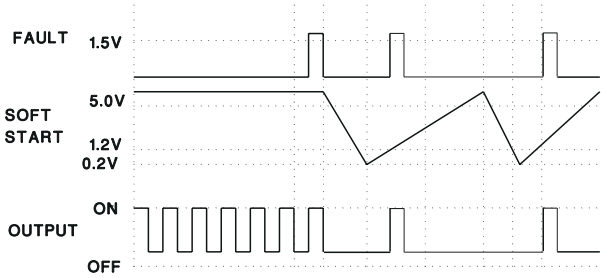

Figure 21.

current limit comparator but not the overcurrent comparator. This would result in brief high power dissipation durations in the main converter at the switching frequency. The intent of the overcurrent comparator is to reduce the effective retry rate under these conditions to a few milliseconds, thus significantly lowering the short circuit power dissipation of the converter.

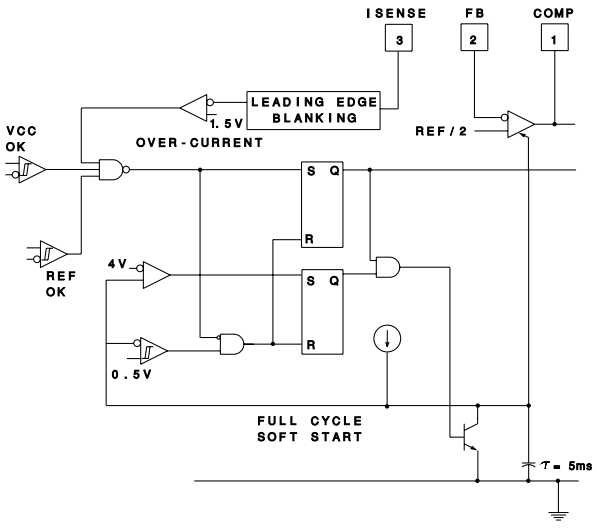

Figure 20.

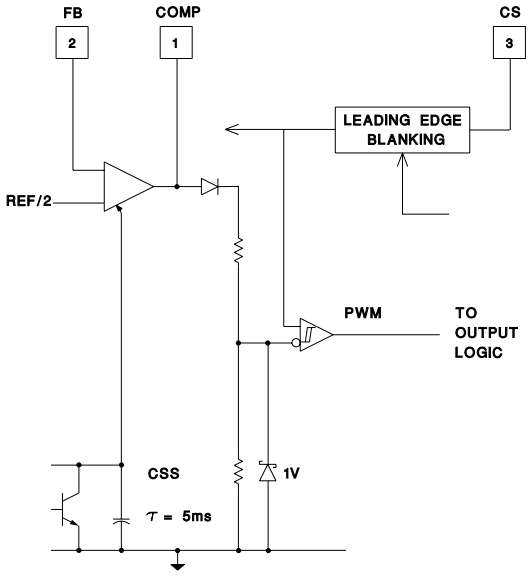

Figure 22.

SOFT START

Internal soft starting of the PWM output is accomplished by gradually increasing error amplifier (E/A) output voltage. When used in current mode control, this implementation slowly raises the peak switch

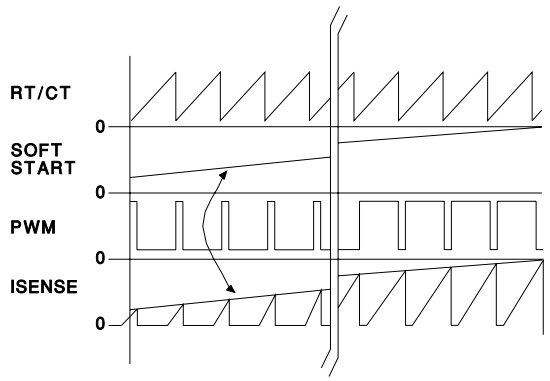

Figure 23.

current each PWM cycle in comparison, forcing a controlled start-up. In voltage mode (duty cycle) control, this feature continually widens the pulse width.

The soft start capacitor (Css) is discharged following an undervoltage lockout transition or if the reference voltage is below a minimum value for normal operation. Additionally, discharge of Css occurs whenever the overcurrent protection comparator is triggered by a fault.

Soft start is performed within the UCC3800/-1/2/3/4/5 devices by clamping the E/A amplifier output to an internal soft start capacitor (Css) which is charged by a current source. The soft start clamp circuitry is overridden once Css charges above the voltage commanded by the error amplifier for normal PWM operation.

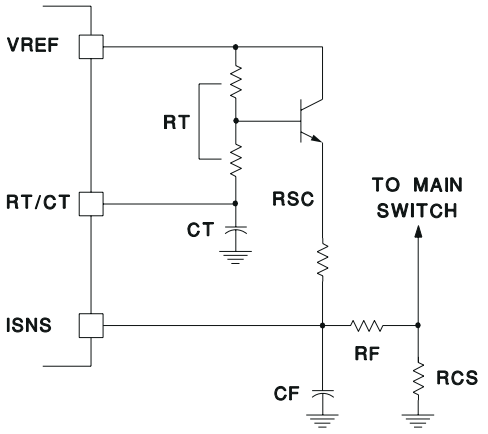

Figure 24: Adding slope compensation.

APPLICATIONS SECTION: CURRENT MODE CONTROL

Peak current mode control is obtained by feeding the converters switch current waveform into the current sense (Isens) input of a UCC3800/1/2/3/4/5 device. The sense resistor should be selected to develop a 0.9 V peak amplitude at full load, including slope compensation. Because of the internal 100 ns typical leading edge blanking, the traditional resistor-capacitor (Rf/Cf) filter to suppress the turn-on noise spike may not be needed.

SLOPE COMPENSATION

Slope compensation can be added in all current mode control applications to cancel the peak to average current error. Slope compensation is neces-

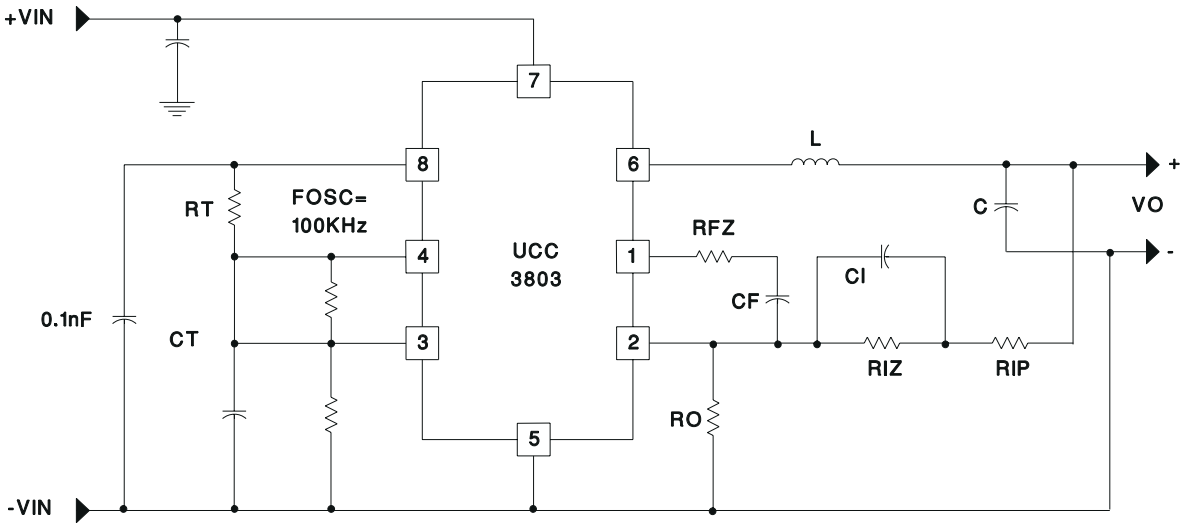

Figure 27: Low-power buck PWM example using on-chip power FETs.

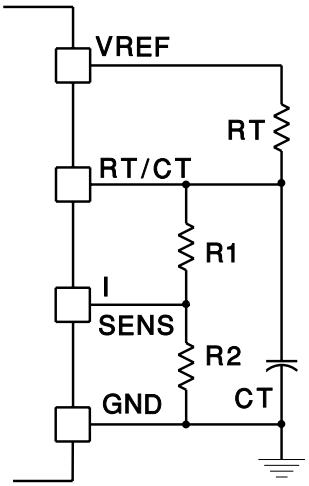

Figure 25: Connecting UCC3802 for voltage mode.

sary with applications with duty cycles exceeding 50%, but also improves performance in those below 50%.

Primary current is sensed using resistor Rcs in series with the converter switch. The timing resistor can be broken up into two series resistors to bias up the NPN follower. This is needed to provide ample compliance for slope compensation at the beginning of a switching cycle, especially with continuous current converters. A NPN voltage follower drives the slope compensating programming resistor (Rsc) to provide a slope compensating current into Cf.

VOLTAGE MODE OPERATION

Any current mode control IC can be used as a direct duty cycle control (voltage mode) by applying a sawtooth ramp to the current sense input. The exponential charging of the timing capacitor (Ct) is used as an approximation of a sawtooth.

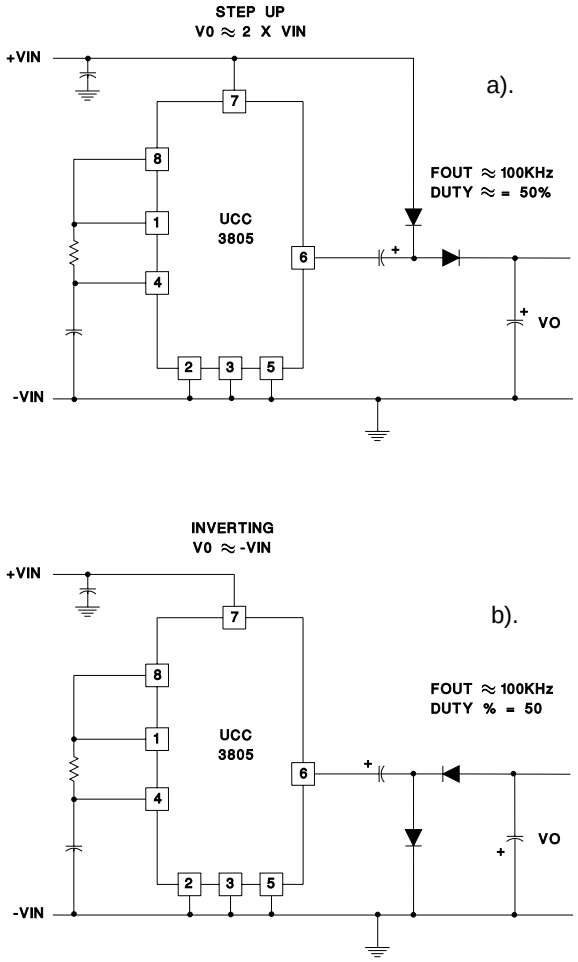

Figure 26: a) Using the UCC3805 to double VIN.
b). Using the UCC3805 to create Vo = –VIN.

The oscillator waveform is resistively divided down by R1 and R2 to a 0.9V maximum amplitude and fed into the current sense input for duty cycle control. A small capacitor across R1 might be necessary to completely bring the current sense input to

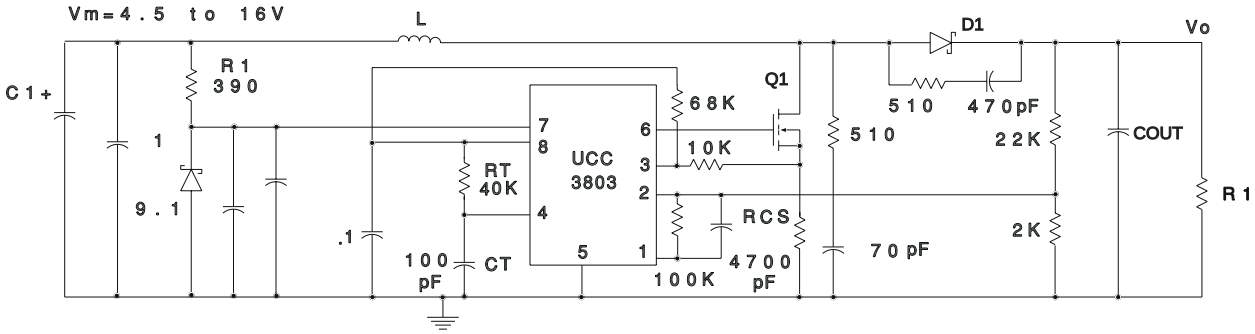

Figure 28: A practical boost PWM example.

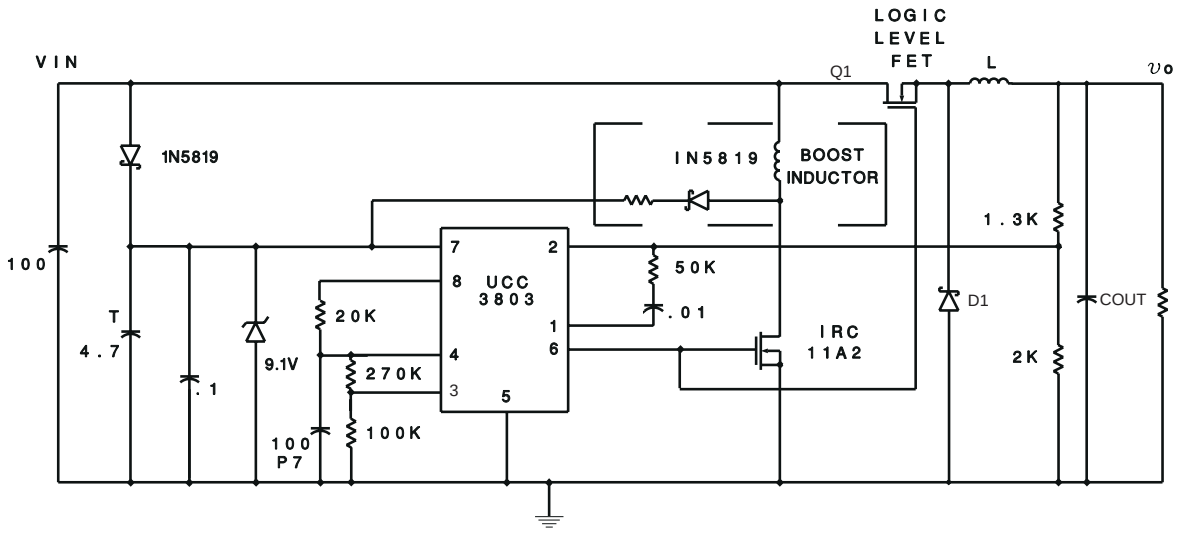

Figure 29: A practical buck PWM that runs with VIN ≥ 4.1V.

zero volts at the beginning of each PWM cycle. Current in the divider network should be kept around 50 microamps, a compromise between low power consumption and good noise immunity. A 15K ohm and 30 K ohm are used in the example.

This circuit can also be used to program the PWM maximum duty cycle. Values should be calculated to attain the 0.9V current sense voltage at the desired maximum duty cycle.

LOW POWER DC/DC CONVERTERS CHARGE PUMP CONVERTERS

Charge pump converters are popular for simple, low power applications. The two basic applications are free running step-up and inverting switchers which use few external components as shown in figure 26.

LOW POWER BUCK REGULATOR

For voltage step down applications, the UCC 380x totem pole output can be used as both the switch and commutating diode of the buck regulator (see figure 27). Power dissipation and the one amp peak current rating of the IC's output stage limit the range of applications to less than 1 amp of output current. High frequency operation permits the use of small and inexpensive surface mount components.

BUCK-BOOST CONVERTER for VOLTAGE STEP-UP and/or STEP-DOWN APPLICATIONS

A two-switch buck-boost converter can be controlled by the UCC380x family of PWMs. This specific

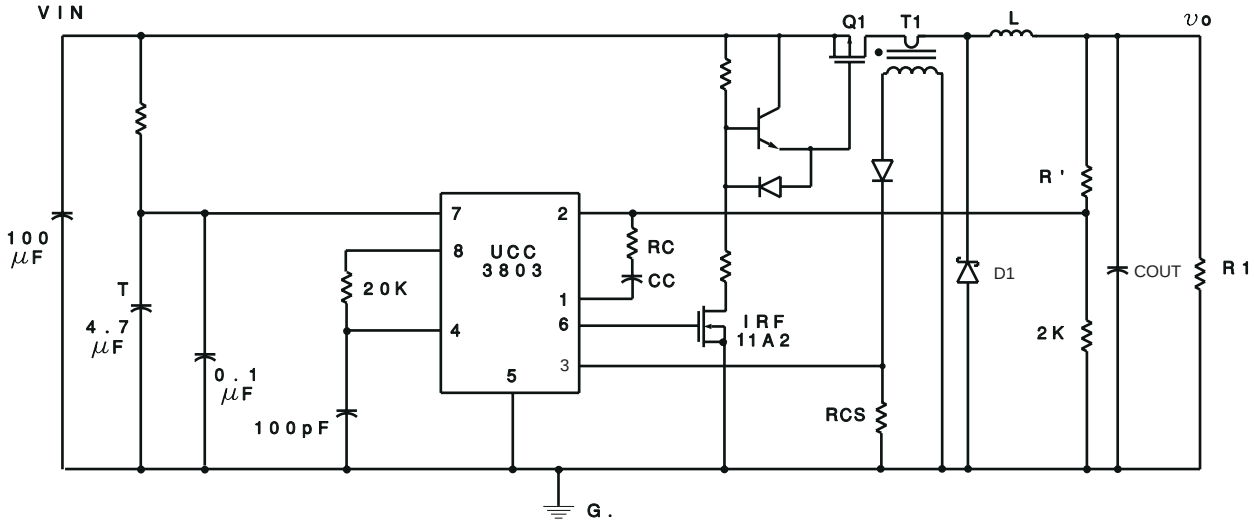

Figure 30: Buck PWM using a PMOS high-side switch.

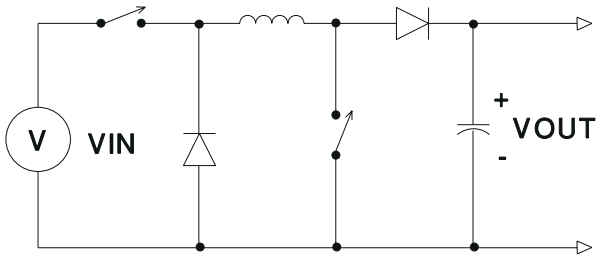

Figure 31. Simplified two switch buck/boost converter drive switches together.

converter is useful in applications where the input voltage can be both higher and lower than the desired output voltage. Implementation combines the voltage step-down characteristic of the buck regulator with the voltage step-up of the boost converter. Both switches are driven simultaneously with this adaptation to simplify the control algorithm. Note that the PWM output of the IC will be used directly for the high side switch in a low power application thus requiring only one external switch. Also, the body diode of the lower side totem-pole output is used as one of the commutating rectifiers, further reducing complexity. As shown in figure 31, this approach is ideal for low voltage, low power DC to DC applications. Higher voltage and higher power applications will require the use of discrete semiconductors for the high side switch and lower diode.

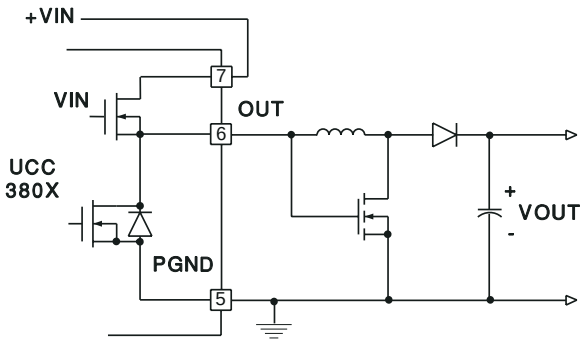

Figure 32. Buck/boost PWM for low power systems.

Duty cycle is varied with input line voltage to provide a regulated output. This non isolated buck-boost converter can be operated in either the discontinuous and continuous inductor current modes. High frequency switching permits the use of very small and inexpensive surface mount inductors for most low power applications. The converter can be controlled by duty cycle modulation (voltage mode) or current mode control, and with or without overcurrent protection.

BOOST CONVERTERS

The UCC 3803 and UCC 3805 devices are fully operational from a 4.5 volt input supply and are ideally suited for 5VDC and battery input PWM boost converter applications. MOSFETs featuring “logic level” gate thresholds are the most likely candidates for the PWM switch as opposed to using standard devices which typically require a gate voltage near 12 volts to be fully on. Currently, many popular N channel MOSFETs are available with logic level gate inputs as an option. Note that many logic level FETs have maximum gate voltage ratings of +/- 10V as opposed to +/- 20V for most conventional FETs which limits their application. Also note that the UCC 380x devices will require a current limited supply when used above 12 volts from a low impedance source.

A basic current mode controlled boost converter application circuit is shown in figure 28. Typical component values for 250 kHz operation are listed in the following tables for a 12V and 24V output applications. The boost converter design equations are summarized below.

BOOST DESIGN SUMMARY:

(Discontinuous inductor current)

$$Vout = Vin \times \left(\frac{t(on)}{t(off)} + 1 \right)$$

$$Iin = Iout \times \left(\frac{t(on)}{t(off)} + 1 \right)$$

$$Ip = 2 \times Iin \times \{ \frac{t(period)}{t(on)}$$

$$Ip = \frac{2 \times t(period) \times Iout \times (t(on) + t(off))}{[t(on) \times t(off)]}$$

$$where\ t(period) = \frac{1}{F(switching)}$$

$$L = \frac{Vout\ minus\ Vin\ (min) \times t(off)]}{Ip}$$

$$C\ out = \frac{(Ip \times t(off)\ max)}{2 \times dVout}$$

$$ESR\ (max) = \frac{dVout}{Ip}$$

BOOST CONVERTER DESIGN TABLE 1

VIN = 4.5 to 10 VDC

VOUT = 12 VDC

IOUT = 0.2, 0.4, 1 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	**3W**	**6W**	**12W**
D1	1A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	12uH	6.8uH	1.8uH
PCH-	27-123	27-682	27-182
Cout	100uF	300uF	500uF
Rcs(ohm)	0.1	0.05	0.033
Q1*	2A/50V RFL2NO5L	IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESl.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 2

VIN = 4.5 to 10 VDC

VOUT = 24 VDC

IOUT = 0.1, 0.2, 0.5 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	**3W**	**6W**	**12W**
D1	1A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	12uH	6.8uH	3.9uH
PCH-	27-123	27-682	27-392
Cout	100uF	200uF	500uF
Rcs(ohm)	0.1	0.05	0.033
Q1*	2A/50V RFL2NO5L	8A/50V IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESl.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 3

VIN = 10 to 18 VDC

VOUT = 24 VDC

IOUT = 0.1, 0.2, 0.5 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	**3W**	**6W**	**12W**
D1	1A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	22uH	12uH	3.9uH
PCH-	27-223	27-123	27-392
Cout	100uF	200uF	500uF
Rcs(ohm)	0.2	0.1	0.066
Q1*	3A/60V IRFF113	3A/60V IRFF113	IRFF133

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESl.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

BUCK REGULATOR

The buck regulator is a more difficult design challenge than the boost converter due to the high side switch. A transformer coupled gate drive is typically required to deliver drive pulses to the switch, which requires about ten volts above the input voltage for proper drive. Current mode control further complicates the design by requiring a current transformer to level shift the high side current sense signal down to the ground based input of the IC. In many applications, direct duty cycle control (voltage mode) can be used to simplify the design although overcurrent protection is lost with common ground applications.

Several examples of common buck regulator application circuits are shown in figures 29 and 30. Direct duty cycle control is used for simplicity, however current mode control can be easily adapted as shown in the example. Tables listing component values and typical part numbers have been included.

DESIGN EQUATIONS:

*Vout = Vin * D (duty cycle)*

$$where\ D = \frac{T(on)}{T(period)}$$

$$L = Vout \times \frac{t(off)}{d\ Io}$$

where: Delta Io is the inductor ripple current and equal to one-half of the minimum output current. Minimum output current has been selected as 10% of the full load current

$$Ipk = Io + \frac{d\ Io}{2}$$

*Iin(DC) = Iout * D*

$$Cout = \frac{d\ Io}{(8 \times F \times d\ Vout)}$$

where F is the switching frequency and Δ Vout is the output ripple voltage

BUCK REGULATOR DESIGN TABLES

TABLE 4

VIN = 4.5 to 10 VDC

VOUT = 3.3 VDC

IOUT = 1, 3 and 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	**1A**	**3A**	**5A**
D1	3A/20V 1N5820	6A/40V 6TQ045	12A/45V 12TQ045
L	39uH	22uH	6.8uH
PCH-	27-393	45-223	45-682
Cout	2uF	4.7uF	10uF
Q1*	8A/60V IRLZ14	8A/60V IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESl.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 5

VIN = 10 to 18 VDC

VOUT = 5 VDC

IOUT = 1, 3 and 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	**1A**	**3A**	**5A**
D1	3A/40V 1N5822	6A/40V 6TQ045	12A/40V 12TQ045
L	120uH	39uH	22uH
PCH-	27-1243	45-393	45-223
Cout	2uF	5uF	10uF
Q1*	4A/50V IRF9Z12	8A/50V IRF9Z22	12A/50V IRF9Z30

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESl.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 6

VIN = 10 to 18 VDC

VOUT = 9 VDC

IOUT = 1, 3, 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	**1A**	**3A**	**5A**
D1	3A/40V 1N5822	6A/40V 6TQ045	12A/40V 12TQ045
L	39uH	12uH	6.9uH
PCH-	27-293	27-123	27-682
Cout	1uF	3uF	5uF

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESl.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

OFF-LINE APPLICATIONS: FORWARD AND FLYBACK CONVERTERS

Several benefits can be realized in off-line applications by using the low current, UC380x BiCMOS PWM controllers. First, the IC can be powered from a resistor to the rectified input voltage source, eliminating the bootstrap winding. This applies to most low frequency applications (50kHz) where the DC supply current required for the gate drive is low. Soft start of the power supply and delayed restart following a fault requires no external parts. The internal leading edge blanking eliminates filtering of the current sense signal. Also, the ICs undervoltage lockout thresholds, internal Vcc shunt regulator and active low totem pole output eliminate any problematic gate drive operation.

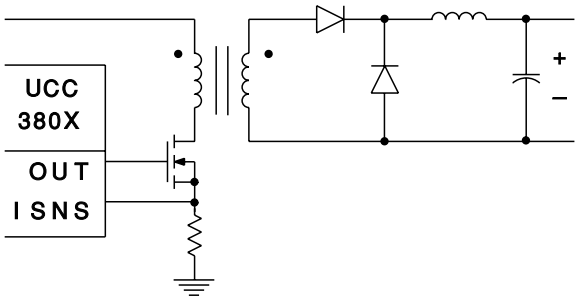

Figure 33. Forward Converter

The basic schematic of a forward converter is shown in figure 33, and a flyback is shown in figure 34. In each, the UCC3804 limits the maximum duty cycle to 50% by internal logic, allowing time for the main transformer to reset. Applications which utilize higher maximum duty cycles, for example 65%, should use the UCC 3802 device without the internal toggle flip flop.

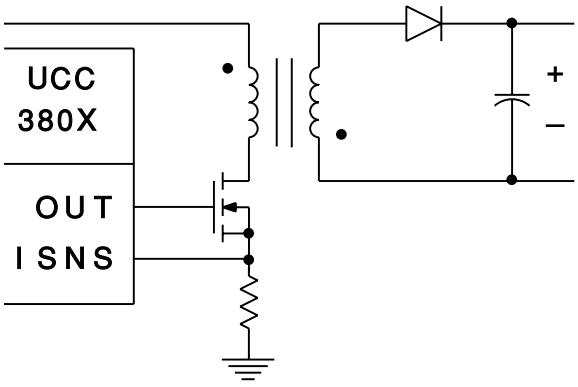

Figure 34. Flyback Converter

UCC380X OTHER APPLICATIONS: UNIVERSAL SYNC GENERATOR

The UCC3803 can be used as a synchronization (SYNC) pulse generator and driver for a variety of applications. Basically, one circuit shown uses the leading edge blanking duration as the SYNC output pulse width. The current limit input is biased at 1.25 volts to terminate the output pulse immediately after the ICs internal blanking pulse width.

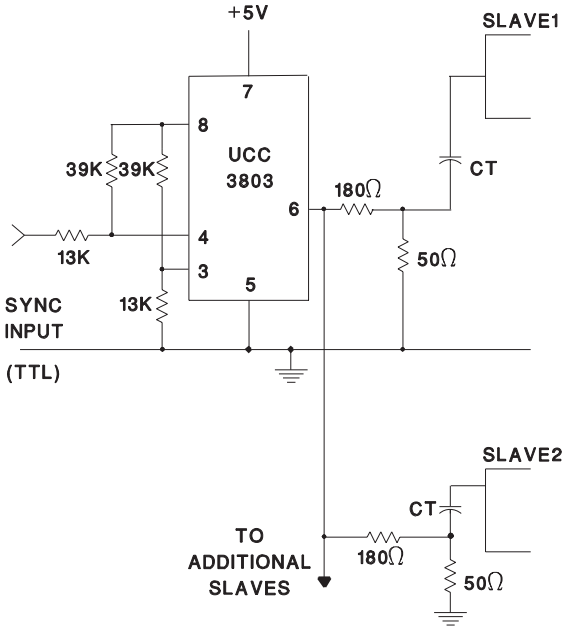

Figure 35. Synchronization Circuit

The oscillator is resistively programmed to a DC level of 1.25 volts also, midway between its upper and lower thresholds. When a TTL compatible SYNC pulse is injected, the amplitude at the oscillator input is raised above its upper threshold. This turns on the internal discharge circuitry which pulls the pin to about 0.2 volts, crossing the lower oscillator threshold. Once this occurs, the discharge transistor is turned off and the ICs output is turned on, generating the SYNC pulse. Note that the current sense input is biased to turn the ICs output off following the leading edge blanking duration, which is used to program the SYNC output pulse width. This 100 nanosecond duration is ideal for synchronizing most PWMs used today with the technique shown.

This circuit can be adapted to generate other width pulses with minor modifications. A capacitor can be added across the lower resistor in the divider network to the current sense input for extending the pulse width. Note that the voltage must be limited below 1.4 volts or a full cycle soft start will be incurred. Also, this capacitor must be discharged before the beginning of each pulse for proper timing

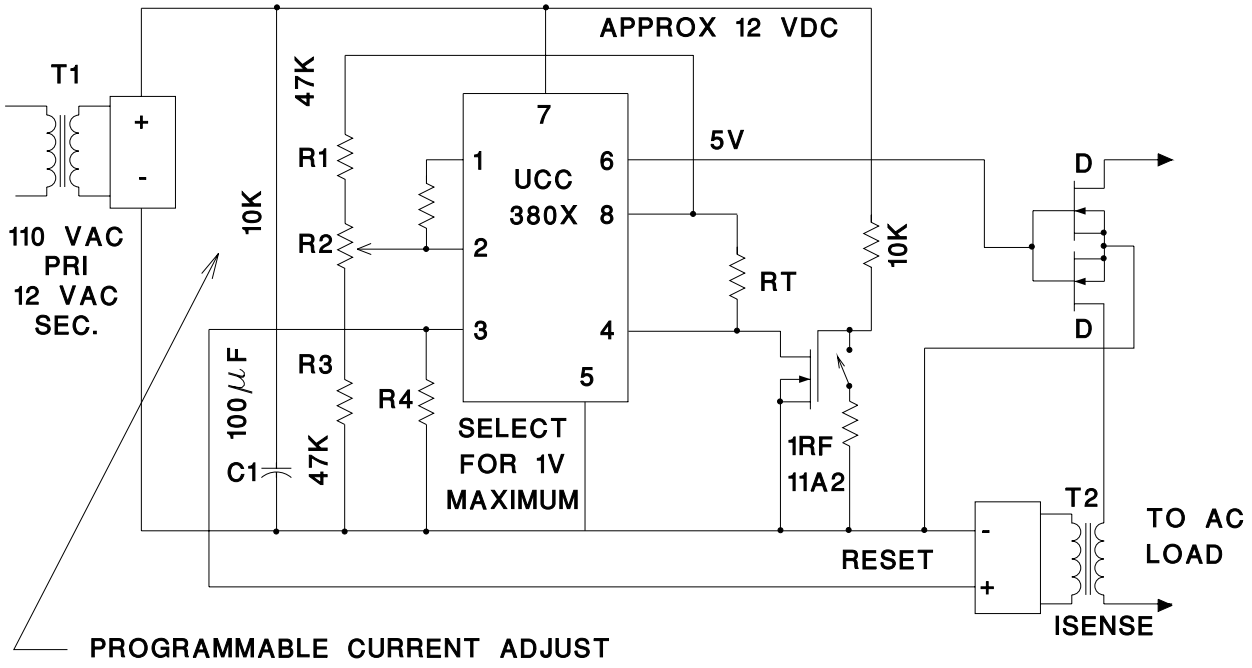

Figure 36. Electronic circuit breaker application.

to occur. One recommendation is to diode couple the current sense input to the oscillator Rt/Ct pin. External circuits can also be used for more precise programming.

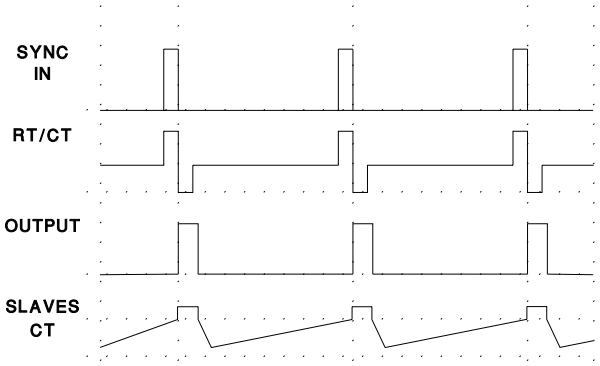

Figure 37. Synchronization Circuit Waveforms

VFO APPLICATIONS

Members of the UCC380x family of devices are adaptable for use in variable frequency applications. The most direct means of accomplishing this is to vary the charging current to the oscillator timing capacitor. Note that the minimum compliance voltage of the current source must exceed the upper oscillator threshold of approximately 2.7 volts. The VFO current source can be generated by an external op-amp for general purpose applications as shown.

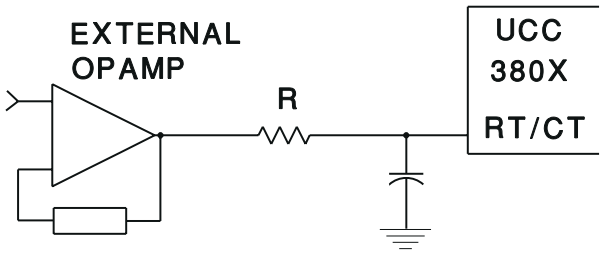

Figure 38. Using UCC380x as a VFO.

Some VFO applications can utilize the ICs internal error amplifier to vary the frequency over a programmed minimum and maximum frequency range. This is done by programming the minimum frequency by a resistor to Vref. Another current sink/source is formed by a resistor to the E/A output. This arrangement performs frequency modulation as the E/A output voltage is varied. Applications which require a fixed 50% duty cycle at varying frequencies, electronic ballasts, for ex-

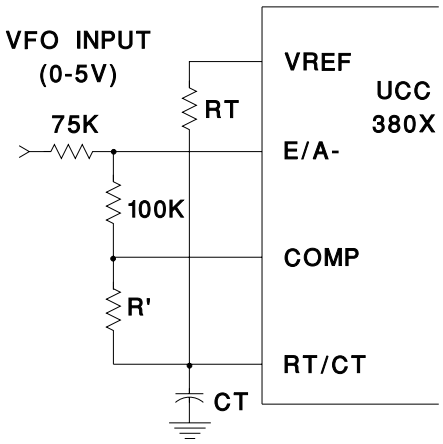

Figure 39: Using the error amplifier to make a simple VFO.

ample, should use the UCC3804 or UCC3805 devices. Output frequency from these will be one-half of the ICs oscillator due to the internal divide-by-two gating circuitry.

FIXED OFF-TIME APPLICATIONS

Obtaining a fixed off-time, variable on-time control technique is easily implemented with the UCC380x family. The oscillator Rt/Ct timing components are used to generate the off-time rather than the operating frequency. Implementation is shown in the corresponding figure 40.

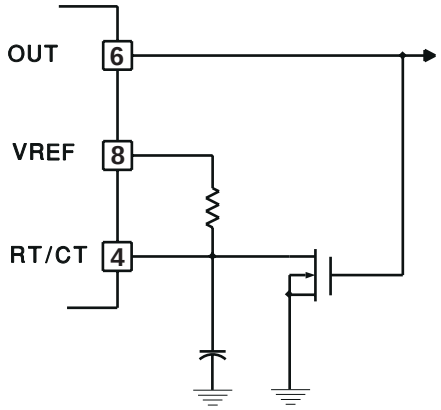

Figure 40: Fixed off-time control.

FULL DUTY CYCLE APPLICATIONS

Any of the UCC380x PWM controllers can be used at full (100%) duty cycle. This mode of operation may be required in certain applications, including DC switch drivers. Implementation requires “freezing” the oscillator so that the output stays high until it is time to turn off. Switch Q1 insures that the PWM output is high when switch Q2 is activated to stop the oscillator. Current limiting can still be accomplished by using the current sense feature of the IC, in addition to modulating the peak current via the error amplifier.

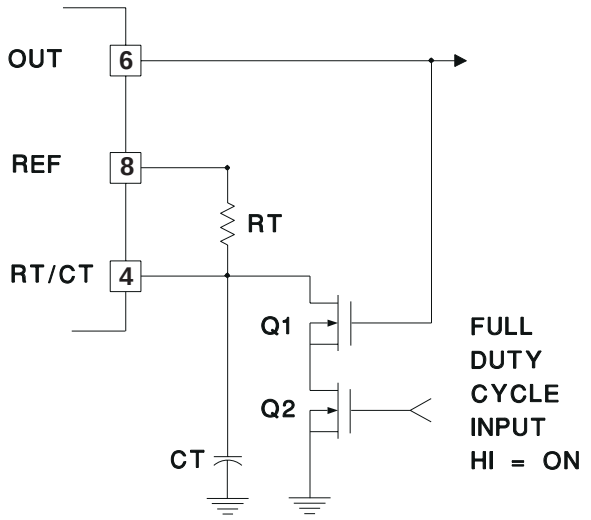

Figure 41. 100% Duty Cycle Circuit

HIGH SPEED, PROGRAMABLE ELECTRONIC CIRCUIT BREAKER

A high speed, programmable electronic circuit breaker can be built using the UCC380x family to perform the control and MOSFET drive functions. Basically, back-to-back power MOSFETS are used as the switching element although an SCR, TRIAC or bipolar switch can also be used. The MOSFETS are connected with the sources tied together to simplify the gate drive while providing a blocking path to current in either direction. Current limiting for an AC supply requires a current transformer, also shown, which can be simplified to a resistor for use in DC input applications. The current sense input to the IC can either be biased up for lower power loss in the current sense network, or programmed by adjusting the error amplifier output voltage to yield a similar result.

SWITCHING COMPONENT NOTES: P CHANNEL MOSFET SWITCHES

Logic level P channel MOSFETs are unavailable today which limits the use of P channel MOSFETs to those with input voltages greater than about ten volts for proper gate drive. The P channel switch will also require a small N channel device to invert its gate drive command, due to the active high output of the PWM (figure 30). High speed PNP transistors are also a suitable choice for some applications.

N CHANNEL MOSFET SWITCHES

Proper gate drive for N channel high side switches will require a supply voltage which is several volts above the input voltage. This is not a problem in five volt input applications using logic level FETs if a nine volt (or higher) supply is also available. If not, one option is to construct a very low power boost converter to generate the nine volt supply to power the IC and gate drive. The boost converter switch can be driven from the UCC380x output which is switching the main output (figure 29). Small, inexpensive surface mount inductors, switches and diodes are readily available. Another possibility is to build a charge pump circuit driven from the PWM output, provided that only a few volts of headroom are required.

GATE DRIVE TRANSFORMER

Higher input voltage applications using high-side switches will require a gate drive transformer due to 12 volt maximum supply rating of the UCC 380x IC family. A small ferrite toroid with two windings and minimal insulation is typically used. A capacitor is placed in series with the primary and is needed for proper reset of the core. The DC offset introduced by the capacitor will effect the primary to secondary turns ratio of the transformer which is dependant on the application. A PULSE Engineering (phone 619-268-2400) model PE-64973 can be employed in most Buck regulator designs.

CURRENT SENSE TRANSFORMER

A current sense transformer is required in the buck regulator application for current mode control. This transformer is used to level shift the current signal from the high side input supply to the ground referenced PWM circuitry. A high turns ratio should be incorporated to reduce power dissipation. Parasitic noise can be minimized by inserting the transformer in series with the drain of the power switch as opposed to its source. A PULSE Engineering (phone 619-268-2400) model PE-64978 current transformer with a one turn primary and 50 turn secondary can be used in most applications.

ADDITIONAL INFORMATION

1. UNITRODE Application Note U-100A;

" The UC3842/3/4/5 Series of Current Mode PWM ICs" :

- UC3842/3/4/5 PWMs
- Applications Information

2. UNITRODE Application Note U-111;

" Practical Considerations in Current Mode Power Supplies" ;

- Fixed OFF-Time Implementation
- Full Duty Cycle
- Paralleling Power Supplies
- Shutdown Techniques
- Slope Compensation (implementation)
- Soft Start
- Synchronization
- Variable Frequency Operation
- Voltage Mode Operation

3. UNITRODE Application Note U-96A

"A 25 Watt Off-Line Flyback Switching Regulator":

- Flyback Converter Design

4. UNITRODE Application Note U-97

"Modelling, Analysis and Compensation of the Current Mode Converter "

- Current Mode Control
- Slope Compensation

5. UNITRODE Design Note DN-42

"Design Considerations for Transitioning from UC3842 to the New UCC3802 Family"

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